Review on Current Conveyor Topologies

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Abstract: Now a day current mode circuits have been receiving significant attention in analog signal processing. For high frequency current mode applications is a current conveyor. Various topologies are used to implement current conveyor circuit. In this paper two topologies are used which are current mirror based topology and differential pair based topology This paper gives the comparison of both topologies in terms of gain, bandwidth, linearity, power consumption.

Keywords: Bandwidth, Gain, CCII, CMOS, Current Conveyor**.**

1. Introduction

The current conveyor is a three terminal device performing many useful analog signal processing functions when the device is connected with other electronic elements in specific circuit configurations. The current conveyor has evolved from first generation to third generation. the first generation current conveyor (CCI) was proposed by Smith and Sedra in 1968 [1] and the more versatile second generation current conveyor (CCII) was introduced by the same authors in 1970 [2] as an extension of their first generation conveyor.

There has been substantial emphasis on the development of current mode signal processing circuits such as filters and oscillators. This is due to increased bandwidth, simple circuitry, better linearity, dynamic range performances and lower power consumption as compared to their voltage mode circuitry. A variety of current mode building blocks are developed with current mode circuits. The current conveyor (CCII) is one among such blocks which has received significant attention. It is hybrid block and has basic construction containing a voltage follower (VF) interconnected with either current mirror or current follower.

2. Literature Review

[1] This paper gives the comparison between two topologies. The first method is inverter based current conveyor and the second method is translinear loop based current conveyor. Second generation current conveyor is used for both the methods. Table gives the comparison of both topologies. [5]

Table 1: Comparisons of Topologies

Sr No	Parameters	Inverter based CCII	Translinear loop based CCII
1	Bandwidth	Twice than Translinear loop based CCII+	Half of the Inverter based CCII+
2	Third Harmonic Distortion	Less	More
3	Output Noise	Less than Inverter based CCII+	More than Inverter based CCII+
4	Area of silicon required	Half	Twice
5	Synthesized by	Analog and Digital	Only Analog

Even through inverter base topology performs better for certain performance measure, it may fail at input voltage dynamic range. The input voltage dynamic range for the CMOS inverter for using in linear application is very narrow; this may lead very small dynamic range.

[2] This paper represents that NMOS differential pair is works, when voltage is greater than 2_{vdsat} and PMOS differential pair is works, when voltage is less than 2_{vdsat}. So using both type of MOSFET, increase in voltage dynamic range is possible. If CCII use only NMOS pair then necessary voltage required is 2_{vdat} to run the circuit. If CCII use only PMOS pair then necessary voltage required, which is less than 2_{vdat} to run the circuit. In this paper, a new circuit is proposed low-voltage low power CMOS rail-to-rail second generation current conveyor. [3]
Drawback: No of transistors increases so power consumption is increases. Power consumption are not compared, however the power consumption for the proposed design seems to be higher because there are two differential pairs and thus requirement of two separate current sources.

[3] The presented active circuit to replace on-chip inductor utilizes a CCII based on active filter.The proposed circuit is able to generate the intended 1V output voltage from a 1.8V input.The conventional buck converter offers an effective technique for on chip integration of voltage regulator. [6]
Disadvantage: The spikes generated by the switching inverter are still visible in the simulation result. To remove this, looking at higher order filters to resolve the issue.It is not suitable for very high impedance load. [6]

3. Circuit Description

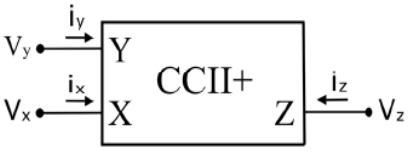

Fig1: Basic CCII+ current conveyor voltages and currents
It is a three port device with the following equations:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Fig 2: Matrix Representation of CCII

Vx = Vy,
Iy = 0,
Iz = Ix,

If a voltage is applied to terminal Y, an equipotential will appear on the input terminal X. An input current I being forced into terminal X will result an equal amount of current flowing into terminal Y. The current I will be conveyed to output terminal such that terminal Z has the characteristics of a current source, of value I with high output impedance. Potential of X being set by that of Y, is independent of the current being forced into port X. Current through port Y being fixed by X is independent of the voltage applied to Y. Terminal Y exhibits an infinite input Impedance.

4. Topologies of Current Conveyor

4.1 Current Mirror Based Topology

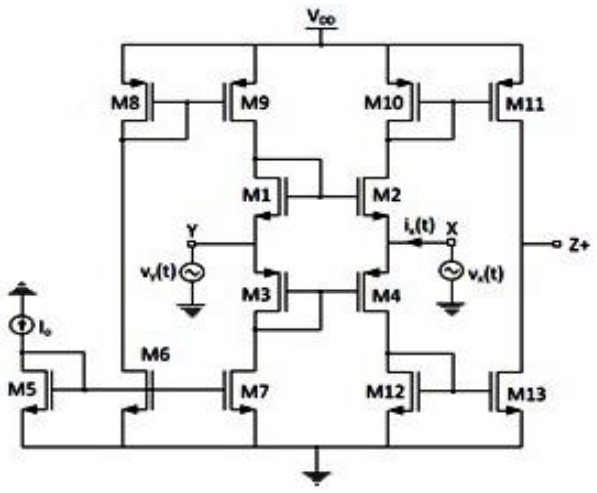

Fig 3: Current mirror based current conveyor [4]

CCII has a mixed translinear loop comprised of two PNP and two NPN transistors. For the positive CCII circuit illustrated in Fig. 3, transistors M1–M4 form the input translinear mixed loop. The current relationship in the loop is characterized by *I1I3 = I2I4*. The circuit is dc biased by *I0*, which is proportional to the current flowing through transistor M1 and M3 (*Io ≈ I1 = I3*). When no load is connected to terminal *X*, the terminal can be considered as low impedance output port. The input port *Y* is considered to be the high impedance node.

4.2 Differential Pair Based Topology

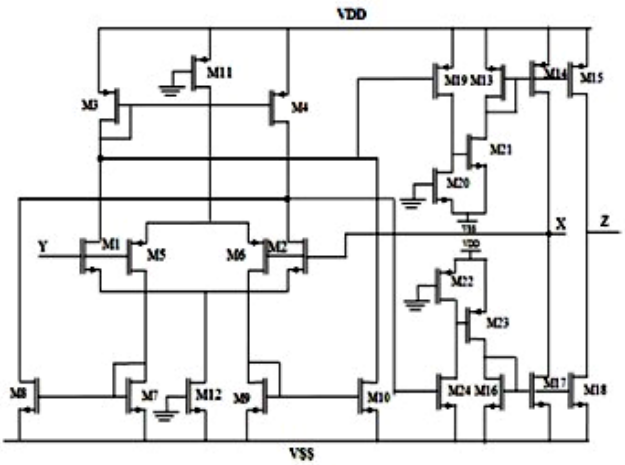

Fig 4: Differential pair based current conveyor [3]

In the input stage, we assembled a NMOS differential pair in parallel with a PMOS differential pair to get a good tracking throughout the supply area. We also duplicated the output stage to minimize the parasitic resistor at X. The operation of this stage can be divided into three regions shown in fig. l. In the positive rail region, only NMOS pair is active. In the mid-rail region both NMOS and PMOS are active, however in the negative rail region only PMOS pair is active.

The input stage is the important part of second generation current conveyor (CCII) to obtain a large dynamic range. This can be achieved by using N-MOS matched differential pair (MI, M2) and another P-MOS matched differential pair (M5, M6) connected parallel to implement the voltage follower between the X and Y terminals. Transistors (M22, M12) provide the necessary biasing currents for each differential pair separately.

5. Simulation Results

5.1 Simulation results of Current Mirror Based Topology

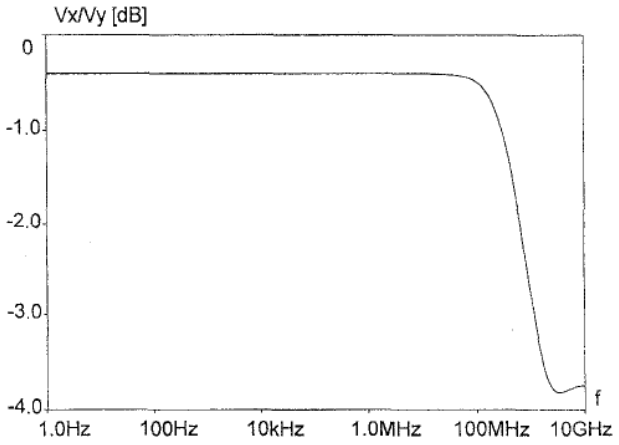

Fig 5: Variation of output voltage as a function of input voltage [11]

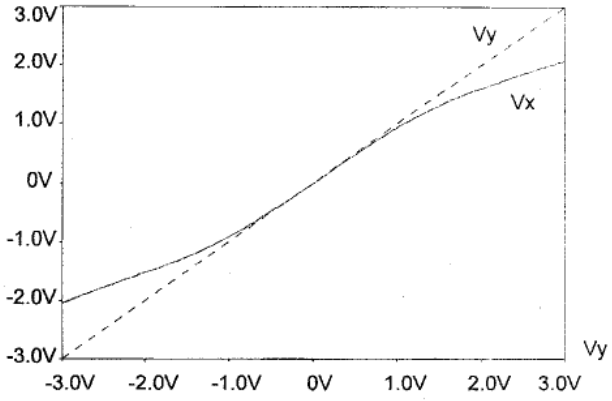

Fig 6: Dynamic Range Representation of Voltage [11]

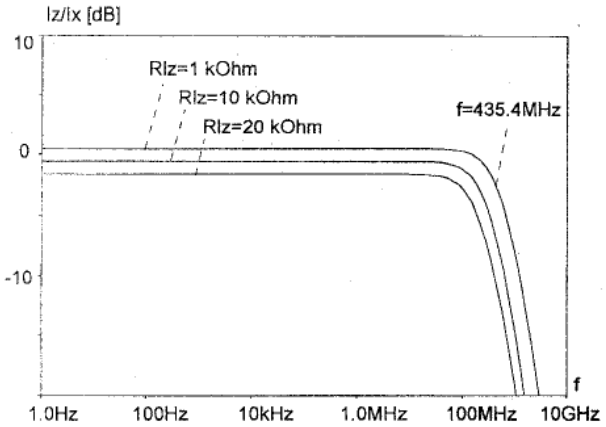

Fig 7: Current gain according to the frequency [11]

5.2 Simulation results of Differential Pair Based Topology

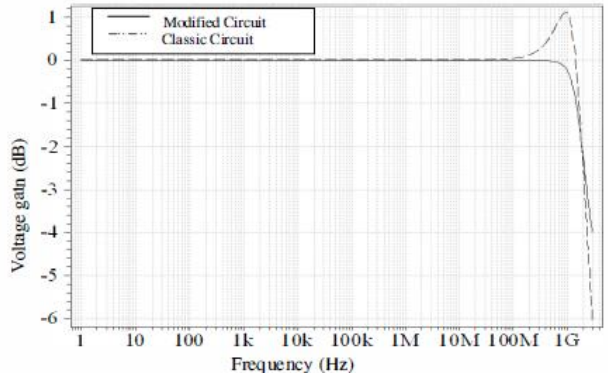

Fig 9: Variation of output voltage as a function of input voltage [4]

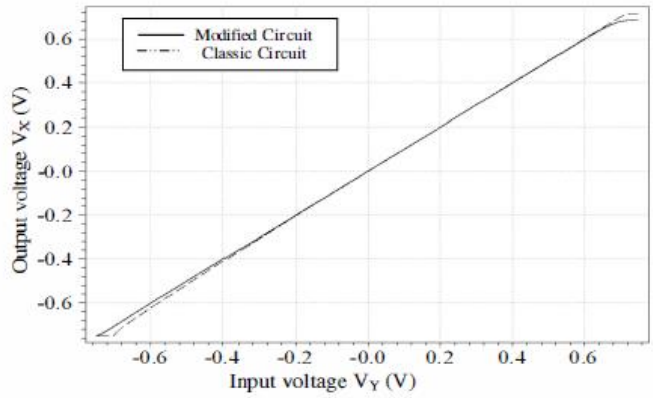

Fig 10: Voltage gain according to the frequency [3]

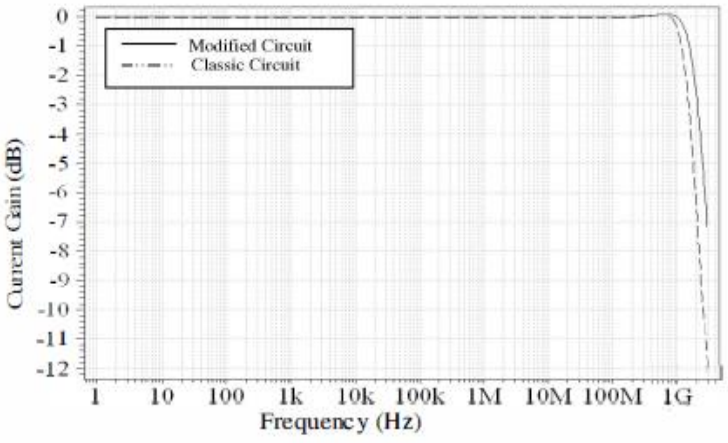

Fig 11: Current gain according to the frequency [3]

6. Conclusion

The effect of CCII topologies performance is evaluated on the basis of gain, bandwidth and linear characteristics. Bandwidth response for voltage transfer is found to be higher in current mirror based topology than differential pair based topology. But in case of linearity and dynamic range differential pair based topology gives better performance than current mirror based topology. Simulations results are compared for both topologies.

References

[1] SEDRA, A.S., and SMITH. K.C.: '*A second-generation current conveyor and its applications*', IEEE Trans. Circuit Theory, 1970, **CT-17,** pp. 132-134

[2] SEDRA, A.S , ROBERTS, G w., and GOHH, F : '*The current conveyor: History, progress and new results*', IEE Proc. G, CircuirsDrvices

[3] Ettaghzouti, Thouraya, NejibHassen, and KhaoulaBesbes. "*Novel CMOS second generation current conveyor CCII with rail-to-rail input stage and filter application.*" Multi-Conference on Systems, Signals & Devices (SSD), 2014 11th International. IEEE, 2014.

[4] Ashenafi, Emeshaw, and MazharulHuqChowdhury. "*Active on-chip voltage regulator based on second generation current conveyor.*" Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on. IEEE, 2013.

[5] Varshney, Garima, et al. "Performance comparison of filter circuits based on two different current conveyor topologies." Signal Processing and Communication (ICSC), 2013 International Conference on. IEEE, 2013.

[6] MazharulHuqChowdhury. "*Active on-chip voltage regulator based on second generation current conveyor.*" Electronics, Circuits, and Systems (ICECS), 2013 IEEE 20th International Conference on. IEEE, 2013.

[7] Abolila, Ahmed HM, Hesham FA Hamed, and El-Sayed AM Hasaneen. "*New±0.75 V low voltage low power CMOS current conveyor.*" Microelectronics (ICM), 2010 International Conference on. IEEE, 2010.

[8] Varshney, Garima, et al. "*Performance comparison of filter circuits based on two different current conveyor topologies.*" Signal Processing and Communication (ICSC), 2013 International

[9] Conference on. IEEE, 2013.

[10] Cha, H-W., and K. Watanabe. "*Wideband CMOS current conveyor.* "Electronics Letters 32.14 (2012): 1245-1246

[11] Popovic, Jelena, Aleksandra Pavasovic, and Dragan Vasiljevic. "*Low-power high bandwidth CMOS current conveyor." International conference on microelectronic*. 1997.

WEBSITE:

[12] https://www.google.co.in/search?newwindow=1&q=cc21+pdf+for+current+conveyor&oq=cc21+pdf+for+current+conveyor&gs_l=serp.3...8446.14619.0.14843.21.21.0.0.0.0.333.3395.0j13j3j1.17.0....0...1c.1.64.serp..16.5.1085.FWeoMSAjCkY